REMARKS

At the time of the Office Action dated May 18, 2005, claims 1-11 were pending. It is noted that paragraph 1 of the Office Action mistakenly states, "[c]laims 1-9 remain pending in the application." An appropriate correction of the record is respectfully requested.

In this Amendment, claims 1, 3 and 5-9 have been amended, and claim 2 canceled. Care has been exercised to avoid the introduction of new matter. Specifically, claim 1 has been amended to include the limitation recited in claim 2. Claim 9 has been amended to be dependent on claim 1. In addition, cosmetic amendments have been made to claims 1, 3 and 5-9. The abstract of the disclosure has also been amended based on MPEP 608.1(b).

Claims 1-9 have been rejected under 35 U.S.C. §102(e) as being anticipated by Tanaka et al.[1]

In the statement of the rejection, the Examiner asserted that Tanaka et al. discloses a layout designing apparatus identically corresponding to what is claimed.

It is well established precedent that the factual determination of lack of novelty under 35 U.S.C. §102 requires the identical disclosure in a single reference of each element of the claimed invention, such that the identically claimed invention is placed into the possession of one having ordinary skill in the art. *See EMI Group N. Am., Inc. v. Cypress Semiconductor Corp.*, 268 F.3d 1342, 60 USPQ2d 1423 (Fed. Cir. 2001); *Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F. 3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994).

[1] Applicants presume that claims 1-11 have been rejected according to paragraphs 12 and 13 of the Office Action, in which the rejection of claims 10 and 11 are discussed. In addition, 35 U.S.C. §102(b) may be appropriate in this case, rather than §102(e) because Tanaka et al. is published one year before the filing date of the present application.

First, Applicants submit that Tanaka et al. does not disclose a logic circuit diagram input device including all the limitations recited in independent claim 1, as amended. Claim 1 recites that "each transistor area calculated by said area calculating means is corrected using an area possession ratio per predefined transistor," which was originally recited in claim 2, now cancelled. It is emphasized that this limitation is not disclosed by Tanaka et al.

In paragraph 4 of the Office Action, the Examiner cited Figs. 14-23; and column 12, line 16 to column 18, line 29 of Tanaka et al., and asserted the limitation recited in claim 2 is disclosed. However, Tanaka et al. does not disclose correcting each transistor area using an area possession ratio per predefined transistor. Tanaka et al., specifically in Fig. 14, discloses "calculating area of transistor involving no diffusion sharing," "calculating area of transistor involving diffusion sharing implemented by folding," "calculating area of transistor involving diffusion sharing implemented by serial connection," and "calculating area of transistor involving diffusion sharing implemented by connection including branch." There is no description regarding the "area possession ration per predefined transistor" in Tanaka et al., and the Examiner did not specifically point out where Tanaka et al. describes that ratio.

Second, Applicants submit that Tanaka et al. does not disclose a logic circuit diagram input device including all the limitations recited in independent claim 3. Specifically, Applicants submit that the reference does not disclose, among other things, the claimed "area holding part" and "area deriving means," recited in claim 3. The claimed "area holding part" is configured for holding standard cell areas for respective instances. The instances each indicate an arrangement condition of each standard cell. The claimed "area deriving means" is configured for deriving areas of the standard cells from the "area holding part" according to the instances respectively corresponding to those standard cells.

In paragraph 5 of the Office Action, the Examiner asserted that Tanaka et al. in Figs. 4 and 5A-5C and their relevant description teaches the claimed "area holding part." According to Tanaka et al., Fig. 4 is a table showing an example of the technology data 32 which includes gate resistance per unit length of a transistor, height of a p-type well, and so forth (see column 8, line 53 to column 9, line 2). Figs. 5A-5C are plain view showing exemplary layouts of transistors (see column 9, lines 3-15). The relationship between the parameters in Fig. 4 and parameters is disclosed in Figs. 5A-5C (see column 9, lines 16-33).

The Examiner also asserted that Tanaka et al. in Figs. 14-23 and their relevant description teaches the claimed "area deriving means." Tanaka et al., specifically in Fig. 14, discloses "calculating area of transistor involving no diffusion sharing," "calculating area of transistor involving diffusion sharing implemented by folding," "calculating area of transistor involving diffusion sharing implemented by serial connection," and "calculating area of transistor involving diffusion sharing implemented by connection including branch."

Based on Applicants' study of Tanaka et al. above, it is apparent that Tanaka et al. is silent on the claimed invention which based on the "instances," holds the standard cell areas in the area holding part, and derives areas of the standard cells from the area holding part.

Based on the forgoing, Applicants submit that Tanaka et al. does not disclose a logic circuit diagram input device including all the limitations recited in independent claims 1 and 3 within the meaning of 35 U.S.C. §102(e). Therefore, Applicants respectfully solicit withdrawal of the rejection claims 1 and 3, and favorable consideration thereof. It is also note that dependent claims 4-11 are patentable at least because they include all the limitations recited in independent claims 1 and 13, respectively.

Conclusion.

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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